at least one controlled gate which delays the propagation of a value generated by a first one of the adapters into a second one of the adapters.

REMARKS

The present application contains claims 1-53. Claims 42-53 are new. Claims 1 and 14 are amended.

Claims 1-32 and 41 stand rejected under 35 U.S.C. §103(a) as being obvious over either Fettweis or Schwartz in view of van der Wal. According to the Examiner, it would be obvious to use variable delay elements (considered by the Examiner as controlled gates) described by van der Wal to delay the propagation of signals in a wave digital filter.

Claim 1 was amended to state that the delay is performed without affecting the result value provided by the wave digital filter. An additional amendment to claim 1 erases the statement that the controlled gate delays the propagation of the value into at least one input of the adapter and adds the possibility that the controlled gate is within an adapter. This additional amendment was made in order to clarify that which was implicit in the claim, that the controlled gate may be located within an adapter and is not necessarily located between two adapters. If this amendment affects the scope of the claim, it broadens the claim.

It is noted that amended claim 1 is broader than original claim 15 and is now traversed as the rejection of original claim 15.

Fettweis describes registers that store signals generated by the adapters. These registers delay the propagation of signals, but the delay affects the result of the wave digital filter. The patent of van der Wal describes (column 6, lines 20-34) variable delay elements that delay the values of IN1 and IN2 so that their horizontal and vertical signals are closely synchronized (column 6, lines 13-14). Applicants respectfully submit that the synchronization is required in order to prevent errors, and hence affects the result value of the filter. Thus, neither of the combined references teaches the limitation that the delay is performed without affecting the result value provided by the wave digital filter. As the combined references are missing one of the limitations of claim 1, applicant respectfully submits that a *prima facie* case of obviousness was not established regarding amended claim 1 of the present application.

Dependent claims 2-19 and 41-44 are allowable at least because they depend on an allowable claim. In addition, the dependent claims add further patentability over van der Wal. The Examiner did not state, why many of these claims are obvious, in his opinion.

Claim 4, for example, requires that the at least one controlled gate is opened when the value it delays is expected to be valid. The Examiner did not state where van der Wal suggests this restriction. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 4.

Claim 5, for example, requires that the value delayed by the at least one controlled gate is required with other values for performing a function and that the controlled gate is opened when all the values required for performing the function are expected to be valid. The Examiner did not state where van der Wal suggests this restriction. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 5.

Claim 7, for example, requires at least one delay unit which delays the propagation of a value into an input of one of the adapters for a predetermined time. The Examiner did not state where van der Wal suggests this restriction. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 7.

Claim 9, for example, requires that the at least one delay unit comprises at least one uncontrolled delay element. The Examiner did not state where van der Wal suggests this restriction. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 9.

Claim 11, for example, requires that the value whose propagation is delayed for the predetermined time comprises a valid value. The Examiner did not state where van der Wal suggests this restriction. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 11.

Claim 14, for example, requires that the value delayed from propagating into the adapter is received from a different adapter. The Examiner did not state where van der Wal suggests this restriction. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 14. Applicant notes that new claim 53 presents the subject matter of claim 14 in independent form. Applicant further notes that the variable delay elements of van der Wal, are located at an entrance to an adder leading to an image filter, which is totally different in purpose and structure from a wave digital filter. The Examiner did not state why the delay elements of van der Wal are relevant to claim 14 of the present application.

Claim 41, for example, requires that the at least one controlled gate delays the propagation of the value until a predetermined number of changes in the value occur. The Examiner did not state where van der Wal suggests this restriction. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 41.

New claim 44, for example, requires that the wave digital filter has only a single external input. Applicant notes that the delay element of van der Wal is used to align two inputs of a single unit and therefore would be useless in a wave digital filter having only a single external input.

Claim 20 requires at least one delay unit which delays the propagation of a first value into at least one input of at least one of the adapters such that the first value is received substantially concurrently with a second value at another input of the adapter. The Examiner did not indicate where this requirement is suggested by any of the cited references. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 20.

Claim 23 requires delaying an input until its value is valid and providing the valid value to an adapter. The Examiner did not indicate where this requirement is suggested by any of the cited references. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 23.

Claim 29 requires delaying a value on a first input until a valid value is received on a second input of an adapter. The Examiner did not indicate where this requirement is suggested by any of the cited references. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 29.

Dependent claims 21, 22, 24-28, 30-32 and 45-52 are allowable at least because they depend on an allowable claim. In addition, the dependent claims add further patentability over van der Wal. The Examiner did not state, for any of these claims why they are obvious.

Claim 24, for example, requires that providing the input comprises providing an input which carries a result from a different adapter. The Examiner did not indicate where this requirement is suggested by any of the cited references. Therefore, the Examiner did not establish a *prima facie* case of obviousness with regard to claim 24.

In view of these remarks, applicant respectfully submits that a *prima facie* case of obviousness was not established regarding claims 1-32 and 41-53 of the present application. Applicant further notes that Fettweis comprises a comprehensive overview of WDFs (theory and practice), but does not mention or hint to the present invention. Furthermore, as described in the background of the present application, attempts have been made to reduce the current consumption of WDFs but, to the best of applicants knowledge, did not suggest the present invention.

Applicant respectfully notes that the office action provided by the Examiner did not relate to each claim of the application as required by the MPEP. For example, the Examiner did not state rejection reasons regarding claim 15. This prevents applicant from responding fully to the

Examiner's rejections and may add to the number of office actions required until allowance. Applicant further notes that any rejection of claim 1 formulated by the Examiner would have been suitable for rejection of original claim 15, which is narrower than amended claim 1. Therefore, a subsequent office action including such a rejection should not be made final.

In view of the above remarks, applicant submits that the claims are patentable over the prior art. Allowance of the application is respectfully awaited.

Respectfully submitted,
D. YELLIN

Paul Fenster

Paul Fenster
Reg. No. 33,877

July 24, 2002
William H. Dippert, Esq.
Reed Smith LLP
599 Lexington Avenue, 29th Floor
New York, NY 10022-7650

Tel.: (212) 521-5400

MARKED-UP CLAIMS

1. (Amended) A wave digital filter, comprising:

a plurality of memoryless adapters each having two or more ports, each port comprising an input and an output; and

at least one controlled gate which delays the propagation of a value into or within ~~at least one input of~~ at least one of the adapters, without affecting a result value provided by the wave digital filter.

14. (Amended) A filter according to claim 1, wherein the value delayed from propagating into or within the adapter is received from a different adapter.